REMARKS

Reconsideration and withdrawal of all grounds of objection and rejection, and allowance of all the pending claims are respectfully requested in light of the above amendments and the following remarks. Claims 1-20, as amended, remain pending herein.

The Abstract has been provided on a separate page to overcome the objection thereto.

In compliance with the Examiner's request, Applicant has changed the title of the invention to "**ELECTRONIC CIRCUIT FOR REDUCING PIPELINE STAGES DEPENDENT UPON INSTRUCTIONS BEING EXECUTED**" which is more descriptive of the claimed subject matter.

Claims 1 and 13 stand rejected under 35 U.S.C. §103(a) over Hennessey *et al.* (*Computer Organization and Design: The Hardware/Software Interface*) ("Hennessey"). Claims 1-20 stand rejected under 35 U.S.C. §103(a) over Hennessey in view of Colwell *et al.* (U.S. 5,604,878) ("Colwell"). Applicant respectfully traverses this ground of rejection for the reasons indicated herein below.

Applicant has amended claims 1 and 13 to recite in part that:

> wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled ~~adapted~~ to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode comprising a truncated passage when processing a second type of instruction when processing a second type of instruction in which the enable

signal is overridden by the control signal so that the latch is held open ~~so that~~for the instruction to ~~propagates~~propagate through the first and second pipeline stages without being stored in the latch;

Support for the above amendments is found in the specification at least at page 6, lines 4-20, and page 7, lines 14-20.

Applicant respectfully submits that the Hennessey, or the combination of Hennessey and Colwell clearly do not disclose, suggest, or in any other way would have rendered claims 1 and 13 obvious at the time of invention, as the combination is clearly silent with regard to a control signal based upon a latency period of each respective instruction, and a reduced mode comprising a truncated passage, wherein the control signal overrides an enable signal, as recited in claims 1 and 13. Nor would the recitations in claims 1 and 13 have been obvious at the time of invention as being within the ordinary level of skill in the art (*KSR International v. Teleflex*, 127 S.Ct. 1727, 82 USPQ2d 1385 (2007)).

For at least the above reasons, Applicant respectfully submits that independent claims 1 and 13 would not have been obvious over Hennessey, or the combination of Hennessey and Colwell. Reconsideration and withdrawal of this ground of rejection are respectfully requested.

With regard to claims 2-12 and 14-20, Applicant respectfully submits that these claims are allowable at least for dependency from one of claims 1 and 13, which are believed allowable for the reasons indicated above, and because of an independent basis for patentability.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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